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EXAMINER	
IWASHKO, LEV	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 02/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/731,996	PARTHASARATHY ET AL.	
	Examiner	Art Unit	
	Lev I. Iwashko	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following are quotations of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-12, 14-28, and 30-36 are rejected under U.S.C. 102(b) as being anticipated by Stracovsky et al. (US Patent 6,378,049 B1).

Claim 1. A method comprising:

- determining at least one characteristic of a memory request; *(Column 5, lines 39-44 – Claim that the controller determines a state which is based on characteristic parameters)*
- and selectively leaving an accessed memory page open after a memory access based, at least in part, on the at least one characteristic for the memory request, *(Column 7, lines 26-34 – Describe how the memory page is open after an access which is based on the state of the memory address)*
- to balance memory access latency and bandwidth of a subsequent memory request(s). *(Column 6, lines 6-16 – Describe how latency and bandwidth are balanced)*

Claim 2. A method according to claim 1, wherein the at least one characteristic is determined based, at least in part, on whether the memory request or a subset of memory requests are to a single memory page or to more than one memory page. *(Column 10, lines 44-53 – State the following: "However, in order to track a state of the physical pages in the shared memory 108 having a number of memory banks, for example, a large number of resource tags which would require a large amount of cache*

memory dedicated to the resource tag buffer 114. This would slow the performance of the universal controller 104 since it would require substantial amounts of time to retrieve particular resource tags for particular pages of memory each of which may be located in disparate locations")

Claim 3. A method according to claim 2, wherein the single memory page is left open after a memory access if the memory request or the subset of memory requests is to the single memory page. *(Column 7, lines 26-34 – Describe how the memory page is open after an access which is based on the state of the memory address)*

Claim 4. A method according to claim 2, wherein the single memory page is closed after a memory access if the memory request or the subset of memory requests is to more than one memory page. *(Column 7, lines 52-65 – State that a multi-bank resource (i.e. multiple pages) is accessed, then a memory page is closed)*

Claim 5. A method according to claim 1, wherein the determining at least one characteristic of the memory request is determined based, at least in part, on a type of memory request expected to be received. *(Column 27, lines 55-64 – State that the request controller chooses from different types of requests)*

Claim 6. A method according to claim 5, wherein the type of memory request is an instruction memory request. *(Column 29-35 – Describe how there is an instruction memory request)*

Claim 7. A method according to claim 6, wherein the instruction memory request results in a page management indicator for leaving the memory page open after the memory access. *(Column 17, lines 5-22 – Describe how there is an indicator for the page being open)*

Claim 8. A method according to claim 5, wherein the type of memory request is a data memory request. *(Column 19, lines 51-53 – Disclose a data request)*

Claim 9. A method according to claim 8, wherein the data memory request results in a page management indicator for closing the memory page after the memory access. *(Column 6, lines 65-67 and Column 7, lines 1-7 – State the following: "In this case, in order to carry out the requested command by the processor 102, the page 1 has to be closed (i.e., page 1 is pre-charged), and page 2 has to be activated, and after the activation is complete, the page 2 is read. Therefor, the universal command 212 shown in FIG. 2B, is generated by the universal command generator 110 having the data fields 202, 204 and 206 set to "1" to indicate "perform the associated operation" while data fields 208 and 210 set to "0" indicating "do not perform the associated operation" (i.e., "NOP")")*

Claim 10. A method according to claim 1, wherein the at least one characteristic is determined, based at least in part, on an arbitration scheme. *(Column 8, lines 47-50 – Declare a "group priority selector register 154" (a.k.a. arbitration scheme))*

Claim 11. A method according to claim 10, wherein the arbitration scheme is based, at least in part, on a priority of a memory request. *(Column 8, lines 47-50 – Describe how the scheme is based upon the priority of a request)*

Claim 12. A method according to claim 11, wherein the priority is based, at least in part, on fairness. *(Column 8, lines 50-60 – State the following, which demonstrates fairness: "In this way, a response or request with a higher priority can bypass that of a lower priority when the lower priority request or response cannot be processed in the next clock cycle. In order to prevent what is referred to as livelock, a livelock counter register 156 contains information about the number of consecutive requests (or responses) with the higher priority can bypass requests (or responses) with a lower priority. In this way, the lower priority request (or response) can not be starved for a substantial number of clock cycles.")*

Claim 14. A method according to claim 1, wherein a memory controller receives the memory request. *(Column 2, lines 30-33 – State the following: "A system*

memory controller will process memory access request conflicts, or commands, as determined by the various priorities assigned to the processors and the refresh system")

Claim 15. An apparatus comprising:

- a plurality of memory pages; *(Column 10, lines 44-45 – Declare pages in the shared memory)*
- and a memory controller, coupled with the plurality of memory pages, to analyze at least a subset of received memory requests, *(Column 9, lines 28-30 – State the following: "At 408, the universal controller generates a universal command that is based upon the sequence of operations required to perform the required request")*
- to determine whether to selectively leave an accessed memory page open after a memory access based, at least in part, on whether the memory request(s) are to a single memory page or to more than one memory page. *(Column 10, lines 44-53 – State the following: "However, in order to track a state of the physical pages in the shared memory 108 having a number of memory banks, for example, a large number of resource tags which would require a large amount of cache memory dedicated to the resource tag buffer 114. This would slow the performance of the universal controller 104 since it would require substantial amounts of time to retrieve particular resource tags for particular pages of memory each of which may be located in disparate locations")*

Claim 16. An apparatus according to claim 15,

- the apparatus further comprising a memory to store content, at least a subset of which is executable content; *(Column 6, lines 29-35 – State that the memory stores executable instructions)*
- and a control logic, coupled with the memory, to selectively execute at least a subset of the executable content, to implement an instance of a memory controller. *(Column 5, lines 16-21 – State the following:*

"Another conventional approach to conflict resolution involves decision-making logic incorporated into a controller type device. Unfortunately, the complexity of the decision making logic requires that a substantial amount of time be utilized in performing the actual decision making before the controller can grant access to the shared memory")

Claim 17. An apparatus according to claim 15, wherein the plurality of memory pages is associated with physical elements of synchronous dynamic random access memory. *(Column 6, line 22 – Declares SDRAM)*

Claim 18. An apparatus according to claim 15, wherein the determination to selectively leave an accessed memory page open after a memory access is dynamic. *(Column 7, lines 8-34 – Demonstrate how leaving the page open is a dynamic action)*

Claim 19. An apparatus according to claim 15, wherein a memory controller receives the at least subset of memory requests. *(Column 9, lines 28-30 – State the following: "At 408, the universal controller generates a universal command that is based upon the sequence of operations required to perform the required request")*

Claim 20. A memory controller comprising: (*Column 6 lines 41-45 –Declares a memory controller)*

- a plurality of memory pages; *(Column 10, lines 44-45 – Declare pages in the shared memory)*
- and a page manager, coupled with the plurality of memory pages, to selectively leave an accessed memory page open after a memory access based, at least in part, on at least one characteristic for a memory request. *(Column 7, lines 26-34 – Describe how the universal controller 104 (a.k.a. page manager) selectively leaves a page open)*

Claim 21. A memory controller according to claim 20,

- the memory controller further comprising a memory to store content, at least a subset of which is executable content; *(Column 6, lines 29-35*

– State that the memory stores executable instructions. Column 6 lines 41-45 –Declares a memory controller)

- and a control logic, coupled with the memory, to selectively execute at least a subset of the executable content, to implement an instance of the page manager. *(Column 5, lines 16-21 – State the following: "Another conventional approach to conflict resolution involves decision-making logic incorporated into a controller type device. Unfortunately, the complexity of the decision making logic requires that a substantial amount of time be utilized in performing the actual decision making before the controller can grant access to the shared memory")*

Claim 22. A memory controller according to claim 20, wherein the accessed memory page is associated with elements of synchronous dynamic random access memory. *(Column 6, line 22 – Declares SDRAM)*

Claim 23. A system comprising:

- volatile memory, associated with a plurality of memory pages; *(Column 6, lines 20-25 – Declare a RAM, and all RAM is volatile memory)*
- and a page manager, coupled with the volatile memory, to selectively leave an accessed memory page open after a memory access based, at least in part, on at least one characteristic for a memory request. *(Column 7, lines 26-34 – Describe how the universal controller 104 (a.k.a. page manager) selectively leaves a page open)*

Claim 24. A system according to claim 23, wherein the at least one characteristic for the memory request is determined based, at least in part, on a type of memory request expected to be received from an agent making a memory request. *(Column 27, lines 55-64 – State that the request controller chooses from different types of requests. Abstract, lines 2-3 – Declare a requesting system)*

Claim 25. A system according to claim 23, wherein the at least one characteristic for the memory request or a subset of memory requests is determined based, at least in part, on whether the memory request or the subset of memory requests are to a single memory page or to more than one memory page. *(Column 10, lines 44-53 – State the following: "However, in order to track a state of the physical pages in the shared memory 108 having a number of memory banks, for example, a large number of resource tags which would require a large amount of cache memory dedicated to the resource tag buffer 114. This would slow the performance of the universal controller 104 since it would require substantial amounts of time to retrieve particular resource tags for particular pages of memory each of which may be located in disparate locations")*

Claim 26. A system according to claim 23, wherein the at least one characteristic is determined, based at least in part, on an arbitration scheme. *(Column 8, lines 47-50 – Declare a "group priority selector register 154" (a.k.a. arbitration scheme))*

Claim 27. A system according to claim 26, wherein the arbitration scheme is based, at least in part, on a priority of a memory request. *(Column 8, lines 47-50 – Describe how the scheme is based upon the priority of a request)*

Claim 28. A system according to claim 27, wherein the priority is based, at least in part, on fairness. *(Column 8, lines 50-60 – State the following, which demonstrates fairness: "In this way, a response or request with a higher priority can bypass that of a lower priority when the lower priority request or response cannot be processed in the next clock cycle. In order to prevent what is referred to as livelock, a livelock counter register 156 contains information about the number of consecutive requests (or responses) with the higher priority can bypass requests (or responses) with a lower priority. In this way, the lower priority request (or response) can not be starved for a substantial number of clock cycles.")*

Claim 30. A system according to claim 23, wherein the volatile memory is synchronous dynamic random access memory. *(Column 6, line 22 – Declares SDRAM)*

Claim 31. A storage medium comprising content, which, when executed by a machine, causes the machine to: *(Column 6, line 21 – Declares a memory)*

- determine at least one characteristic of a memory request; *(Column 5, lines 39-44 – Claim that the controller determines a state which is based on characteristic parameters)*
- and selectively leave an accessed memory page open after a memory access based, at least in part, on the at least one characteristic for the memory request, *(Column 7, lines 26-34 – Describe how the memory page is open after an access which is based on the state of the memory address)*
- to balance memory access latency and bandwidth of a subsequent memory request(s). *(Column 6, lines 6-16 – Describe how latency and bandwidth are balanced)*

Claim 32. A storage medium according to claim 31, wherein the at least one characteristic for the memory request is determined based, at least in part, on a type of memory request expected to be made by an agent making a memory request. *(Column 27, lines 55-64 – State that the request controller chooses from different types of requests. Abstract, lines 2-3 – Declare a requesting system)*

Claim 33. A storage medium according to claim 31, wherein the at least one characteristic for the memory request or a subset of memory requests is determined based, at least in part, on whether the memory request or the subset of memory requests are to a single memory page or to more than one memory page. *(Column 10, lines 44-53 – State the following: "However, in order to track a state of the physical pages in the shared memory 108 having a number of memory banks, for example, a large number of resource tags which would require a large amount of cache*

memory dedicated to the resource tag buffer 114. This would slow the performance of the universal controller 104 since it would require substantial amounts of time to retrieve particular resource tags for particular pages of memory each of which may be located in disparate locations")

Claim 34. A storage medium according to claim 31, wherein the at least one characteristic is determined, based at least in part, on an arbitration scheme. *(Column 8, lines 47-50 – Declare a "group priority selector register 154" (a.k.a. arbitration scheme))*

Claim 35. A storage medium according to claim 34, wherein the arbitration scheme is based, at least in part, on a priority of a memory request. *(Column 8, lines 47-50 – Describe how the scheme is based upon the priority of a request)*

Claim 36. A storage medium according to claim 35, wherein the priority is based, at least in part, on fairness. *(Column 8, lines 50-60 – State the following, which demonstrates fairness: "In this way, a response or request with a higher priority can bypass that of a lower priority when the lower priority request or response cannot be processed in the next clock cycle. In order to prevent what is referred to as livelock, a livelock counter register 156 contains information about the number of consecutive requests (or responses) with the higher priority can bypass requests (or responses) with a lower priority. In this way, the lower priority request (or response) can not be starved for a substantial number of clock cycles.")*

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 13, 29, and 37 are rejected under 35 U.S.C.103(a) as being unpatentable over Stracovsky et al. as applied to claims 1, 10-11, 23, 26-27, 31, and 34-35 above, further in view of Nishikado et al. (US PGPub 2002/0052798 A1).

Stracovsky teaches the limitations of claims 1, 10-11, 23, 26-27, 31, and 34-35 for the reasons above.

Stracovsky 's invention differs from the claimed invention in that there is no specific reference to a quality of service.

Stracovsky fails to teach claims 13, 29, and 37, which state "A method according to claim 11 (or 27 or 35), wherein the priority is based, at least in part, on quality of service." However, Nishikado states that "The user management information (70) for each user includes user name information (71) indicating a user name, a user password (72) indicating a password for authentication, user attribute information (73) indicating the user attribute such as sex and age, user group information (74) holding names of groups to which the user belongs, and user priority information (75) used to control service quality for the user having the information such as minimum, maximum, and default service priority allowed to the user" (Section 0067, lines 3-11). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Universal Memory Controller" of Stracovsky and Nishikado's "Service System" before him at the time the invention was made, to combine the two inventions so that the priority ranking would be based at least in-part on service quality, so that the system would run efficiently and with good quality.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on M-F (alternating Fridays), from 8-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lev Iwashko

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PRIMARY EXAMINER